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Memorandum 4022

Title: GaAs VARACTOR DIODE MMIC FABRICATION TECHNOLOGY

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ABSTRACT

The design criteria and techniques developed to fabricate a monolithic low series resistance N on N^+ GaAs varactor diode and the associated microwave circuit are described. Details of a high resolution polyimide patterning process developed for this device are included as is a description of the experimental work carried out to establish the practical design rules for the polyimide dielectric on chip capacitors.

A description of the seven level mask set and associated processing are included and an assessment of the yield obtained on several wafers is discussed.

The processing technology described in this memo has been successfully transferred to UK industry.

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GaAs Varactor Diode MMIC Fabrication Technology

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GaAs Varactor Diode MMIC Fabrication Technology

1. Introduction

This circuit was built as a demonstration prototype for subsystem research in DP1 division. Initial experimental work was carried out within DP1 division using hybrid microwave circuits in which PIN diodes switched in fixed value overlay capacitors. This approach indicated that the concept was sound but that, owing to space limitations, the discrete capacitor approach was not capable of being extended to cover the required capacitance range and also allow fine control within that range.

The possibility of using a discrete varactor diode in the hybrid circuit had also been considered by DP1, but it was concluded that the associated bond wire inductances would preclude this. DP2 division were approached at this stage regarding the possibility of producing a suitable monolithic microwave integrated circuit (MMIC) version of the circuit based on a varactor diode operating at X band. This note describes the work carried out within DP2 to develop a suitable fabrication process and realise a number of prototype chips for evaluation. It should be borne in mind that whilst this document fully describes the fabrication processes it does not contain a full description of the circuit layout. This will be described later in a separate document from DP1.

Sections 2 and 3 describe the calculations which defined the overall structure of the IC, and the technology implications of the chosen solution. Section 4 is a description of the process scheme. The dc results obtained from the processed wafers are summarised in section 5. The selected process scheme is assessed in the light of these results in Section 6, and some overall conclusions from the exercise are outlined in section 7.

In general the fabrication scheme for this work was based upon processing techniques which have been in routine use in DP2. However, where particular process improvements were required, a more detailed description of the processing step is provided in this memo together with a summary of any process mapping carried out to identify a usable set of operating conditions.

2. Varactor Diode Specification and Design Philosophy

2(a) Varactor Diode Specification

The diode was required to be of low series resistance, typically 0.5 ohm, with a zero bias capacity of 2 pf and a minimum

capacity of 0.5 pf. The associated microwave circuit would have to incorporate fixed value capacitors of 1 pf and some means of biassing the varactor via an RF Block.

2(b)   Design Philosophy

In order to capitalise on existing technology the materials structure originally considered was based on an N^+ on N on semi-insulating (S.I.) FET type structure (Figure 1). The modelling results obtained, however, showed that this structure would not allow the series resistance target to be achieved. Additional calculation showed that in order to achieve the required resistance an N on N^+ on S.I. materials structure combined with a multifinger diode geometry would be necessary.

A mesa type fabrication route was adopted with all circuit pads, bias lines and associated tracks fabricated on the exposed S.I. substrate. If required these components could be gold plated up to 3 microns thickness. The capacitors would be fabricated using a polyimide dielectric sandwiched between metal layers and the RF blocks on the DC bias lines would use a combination of capacitors and moderately resistive thin gold tracks several mm long.

3.   Technology Requirements

3(a)   Material

As stated earlier an N on N^+ on S.I. structure was necessary with the requirement that the N^+ be at least 1.5 um thick for a doping level of 2×10^{18} per cc. The diode N layer had to be selected so that the series resistance of the undepleted region was small whilst at the same time the diode formed on this layer had to have a high enough reverse breakdown to allow sufficient bias to achieve the 4:1 capacity swing required. A larger capacity swing would require graded diode layers.

An ideal diode fabricated on a 1×10^{17} per cc N layer would be expected to have a reverse breakdown of 15 $V^{(1)}$ and a bias swing between 0 V and -15 V should result in a capacity swing of 4.5:1. The depletion depth at 15 V would be approximately 0.4 micron so an overall layer thickness of 0.5 micron would allow for clean up etches, for example during processing. To achieve 2 pf at zero bias on this layer requires a Schottky area of 2500 square microns.

The N^+ underlayer was required to have a carrier concentration of 2×10^{18} per cc and a practical layer thickness of 2 microns was adopted as a suitable compromise between minimising resistance and the requirements of draping metallisations over tall mesa edges. The material required is shown diagramatically in figure 2.

The large overall thickness of these layers implied grown rather than implanted wafers and the route adopted was MOCVD via the DP4 growth area. This technique was the only one on-site producing

layers routinely to the required specification at the start of this programme. MBE layers were provided by DP4 during the latter stages of this work, but these layers were not processed as the DP1 requirements had by then been fulfilled. The largest wafers which could be processed at the time were half 2" diameter wafers and a number of layers were provided by DP4 on substrates of this size. The Post Office Profile Plotter (POPP) plot of a typical layer is shown in figure 3.

3(b)   Dielectric Overlay

A consequence of the N on N^+ diode structure is the need to isolate any Schottky fingers from contact with the exposed N^+ layer where the fingers run up the sides of mesas. In the absence of an air bridge technology it was decided to use a polyimide overlay referred to as a 'doormat' to allow access between the N diode layer and the S.I. substrate (figure 4).

The patterning requirements on this "doormat" were very stringent in that the position of the edges of the dielectric pads had to be held to better than $\pm$ 1.5 microns in order to maintain the diode capacitance within a 5% tolerance band. To minimise parasitics and provide a degree of planarising over the 3 micron tall mesa edge the polyimide had to be at least 2 microns thick. An additional requirement was that the polyimide, after patterning, had to have sloping edges in order that metal tracks could easily be carried over the regions of dielectric. Previous experience with polyimide patterning indicated that holding pad sizes to better than 10 microns was difficult with our existing technology and an investigation was therefore carried out to improve this [Appendix A].

3(c)   Capacitors

An investigation was already under way to examine capacitor fabrication using a polyimide dielectric and as the polyimide "doormat" patterning process was already incorporated into the proposed fabrication schedule it was decided to combine the two polyimide patterning steps into one process stage. The consequence of this approach was that the thickness of the polyimide and the patterning technique to be used were fixed by the "doormat" requirements. The capacitor investigation was therefore limited to assessing the reproducibility of capacitors made using these techniques and determining the practical dielectric constant for polyimide associated with our particular curing cycle. The details of this work are described in Appendix B.

4)   Description of Photolithographic Mask Set and Fabrication Process

The basic parameters of the MMIC have been discussed in the earlier sections of this report and are summarised here:-

1)   Material: 0.5 um of 1×10^{17} cm^{-3} N GaAs
grown on 2 um of 2×10^{18} cm^{-3} N^+ GaAs
grown on S.I. substrate

2)   Schottky Area: 2500 microns^2

3)   Polyimide dielectric 2 um thick for capacitors and "doormats".

A cross section of the diode is shown in figure 4 and a perspective drawing of the same region is shown in figure 5.   It should be noted that the mesa edge shown is orientation specific and that etch steps at right angles to the step shown will be undercut and not allow metal lines to be draped over them.   This is a consequence of the particular wet etching processes routinely used in DP2, which employ ammonium hydroxide/hydrogen peroxide/water mixtures.

In order to minimise the series resistance as much as possible a multi-finger design was required for the Schottky area and a layout of 10 fingers, each 5 microns by 50 microns was adopted with a corresponding castellated ohmic contact configuration.   The complete diode area is shown in photograph 1.

The usual sequence of fabrication steps is defined as: first, mesa etch, second ohmic contact, last, schottky contact.   The Schottky stage is placed last as, in general, the Ti/Pd/Au Schottky will not survive the 360°C ohmic annealing schedule.   For obvious reasons the polyimide dielectric has to be deposited and patterned before the Schottky stage and as the 300°C polyimide curing cycle is known not to affect the ohmic contacts, the polyimide processing is placed between the ohmic and Schottky stages.   These individual stages will now be outlined in some detail.   A plan view of the major features of each mask layer is provided in Appendix C.   The features used to ensure correct alignment of each masking layer are also described in this appendix.   A step by step listing of the process sequence used is included in Appendix D.

4(a)   <u>Mesa Etches</u>   [Mask 1 and Mask 2]

Two etches are required, each requiring its own mask, one to form isolated mesas of N on N$^+$ material at each device site (figure 6) and a second etch to remove areas of the top N layer and expose the N$^+$ layer for subsequent ohmic contacting (figure 7).   An cverall alignment tolerance of $\pm$ 5 microns was allowed throughout the processing so this second mask was designed to leave a band of N material 10 microns wider than the 5 micron wide Schottky finger and 5 microns longer than the 50 um length.

The etch depth control on the first etch step is not critical provided the step is sufficient to fully isolate the individual device areas from each other.   The criterion adopted in practice is to target for the overall active layer thickness [N plus N$^+$] plus 0.3 microns.

The second etch is more demanding on depth control.   If too much material is removed, the resistance of the Schottky to ohmic path will be increased.   The target in this case is an etch step of N layer thickness plus 0.1 microns.

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At the conclusion of these etching stages the wafer should consist of a large area of exposed SI substrate with single large mesas at each device site. Each mesa should consist mainly of N^+ material and have 10 smaller mesas of N material along its top surface near one edge (figure 8).

4(b)   Ohmic Contacts [Mask 3]

The ohmic contacts are required to interlace with the 10 small N mesas and the castellation dimensions are again based on the 5 micron alignment rule. Each cut out is therefore 10 microns wider than the N mesa width and 5 microns longer, see Photograph 2.

Various circuit elements and the bottom plate of all the capacitors are also formed during this step. The ohmic contact was formed using standard Ge/Au technology, as described in ref. 2.

4(c)   Polyimide [Mask 4]

The polyimide forms the dielectric for all the capacitors at the same time as the dielectric "doormat" is formed. As mentioned earlier the critical requirement is holding the edge of the "doormat" to a total tolerance of $\pm$ 1.5 microns in order to achieve consistent varactor capacitances.

In practice it was not found possible to reliably spin 2 microns of polyimide. A 3 micron layer was, therefore, spun on and either subsequently ashed to remove 1 micron before patterning took place or patterning was performed on the 3 micron layer which was subsequently ashed overall. This latter technique had an additional benefit of rounding the edges of the dielectric pads.

4(d)   Schottky layer [Mask 5]

This mask defines the varactor area and the top plates of all the capacitors. In order to provide a symmetrical layout the capacitors used in the MMIC were designed as series combination pairs ie they were comprised of one top plate which equally overlapped two bottom plates, see figure 9 and photograph 3.

The Schottky connected, by overlaying, to the ohmic metal forming the rest of the circuit. No problems were apparent due to poor adhesion in these areas. The Schottky metal used was a standard thermally evaporated Ti/Pd/Au layer.

4(e)   Au plated layer [Mask 6]

This mask was added after the initial wafers had been processed and was required to enable circuit losses in the 0.8 micron thick circuit elements to be reduced. Using standard techniques and resist thicknesses selected areas could be plated with 3 microns of gold (as described in appendix E).

Optical and SEM pictures of completed devices can be seen in photographs 4, 5, 6 and 7.

5)   Results

This section describes dc measurements carried out on part and fully processed wafers. Rf measurements were carried out by DP1, and will be the subject of a separate memo. A total of four half 2 inch diameter wafers were processed to completion. These are referred to as wafers A to D. Wafers A to C were processed without a final plating step. The need for this stage only became apparent after rf testing the chips from the initial wafers.

Wafer A gave anomalous D.C. results in that it displayed a complete absence of diode characteristics. A simple two probe breakdown test on the exposed GaAs surface on the device side of the wafer indicated the presence of a conducting layer. Comparing the mesa heights with the epi layer thicknesses obtained from the POPP indicated that the mesa etch should have been adequate to fully remove the device layers. A breakdown test on the rear face of the wafer indicated that there was a conducting layer present on that face also. Investigation by DP4 confirmed that although the substrate material was originally semi-insulating, type conversion may have taken place during the growth cycle[3]. This effect had been noticed previously on substrate material from the same batch. Subsequent devices made on layers grown on substrates qualified for ion implantation annealing at 850°C did not exhibit this effect.

In general all devices exhibited much lower reverse breakdowns and, apart from wafer D, higher values of capacity than expected. Although the POPP plots for the wafers showed that there was generally a higher doping level in the N layer than required, this was not sufficient to explain the values of zero bias capacity measured. It was also thought unlikely that end effects in the multifinger structure would account for the discrepancy.

An accurate determination of the, in situ, varactor capacitance proved very difficult as the various fixed capacitors in the surrounding circuit were of similar values to the zero bias junction capacitance and appeared in parallel with it. In order to investigate the varactor in more detail one chip from wafer B and two from wafer D were examined with the external circuit scribed off. Doping profiles deduced from C/V measurements made on these devices are shown in figures 10, 11 and 12.

The results from the device from wafer B indicate an N layer doping level nearly twice that obtained from the original POPP [ie device 4 x 10^{17} per cc, POPP 2.5 x 10^{17} per cc]. The two devices from wafer D show good agreement with the original POPP [devices approx 1.5 x 10^{17} per cc, POPP approx 1 x 10^{17} per cc].

The experimental and theoretical C/V curves for the device from wafer B are shown in figure 13. The good agreement obtained over a range of bias confirming the doping levels obtained from the device measurements. This would then account for the excess capacity values measured on wafer B. It should be noted that all POPPs were carried out on regions scribed from the edges of the half wafers and would therefore be many [> 15] millimetres away from the areas on which the

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devices were fabricated. Edge effects during growth may also be significant as the wafer size is the maximum allowable in the growth kit.

Measurement of the series resistance of the diode was initially estimated by examining the slope of the forward biassed varactor. A value of 2 ohms was obtained on the device from wafer B at a forward current of 25 mA. A more reliable measurement based on curve fitting to the forward biassed diode characteristics gave a value of 1.03 ohms with an associated barrier height of .69 v and an ideality factor of 1.22. This value of resistance is larger than expected and the reason for this has not yet been isolated. The specific contact resistance of the ohmic contacts was checked during processing by using 'drop in' test patterns on the wafers and was found to be as expected[2]. The possibility of extra series resistance in regions of level 1/level 2 metal overlaps was eliminated by probing the diode side of the overlaps. It is believed that a detailed investigation based on the use of simple test patterns would be the only way to satisfactorily resolve this problem.

Of the four wafers processed, the first was a total loss electrically because of the type conversion problem, although it exhibited a very high visual yield. The following discussion of yields applies to the other 3 wafers processed. The design of this MMIC highlighted a major disadvantage associated with physically large chips in that with a potential maximum yield of only 6 or 7 chips per half wafer processed, a very high yield per component is required in order to produce 3 or 4 useful chips per wafer. As described earlier the processing of these devices is complex as each chip contains 3 capacitor pairs, one high precision "doormat" region and 10 Schottky fingers. The yields of these individual components must all be 100% and coincident in order to produce a useful chip. The one advantage of having so few chips per wafer is that it is not too time consuming, at the development stage, to visually inspect all the devices during processing. By adopting this approach after every engraving stage for instance, an accurate assessment of probable yield can be made and hence a decision reached on whether to proceed with a non reversible etch or metallisation step, or strip the resist and repeat the stage. The criterion adopted was to repeat a stage if visual inspection indicated that two or more devices might be lost. As an indication of the severity of this test the finger exposure on one wafer was repeated because of contamination on one finger on two devices, ie a finger yield of 97% [7 devices, 68 out of 70 fingers OK] was inadequate.

On the three wafers processed to DC and RF testing the overall device yield was between 60% and 70%. Some caution must be exercised in interpreting these figures as at least one of these wafers underwent repeat processing at the diode finger patterning stage.

6)   **Process assessment**

The process scheme adopted for this work has been shown to be capable of producing a high yield of components. It is of value to

assess the features of the process which have contributed to this success, and identify areas where further work could usefully assist in consolidating the process to a satisfactory level for the fabrication of a larger volume of components.

Three areas of process monitoring have been adopted which all proved beneficial. Firstly the importance of substrate qualification was highlighted by the total failure of the first wafer. Wafers used subsequently had been qualified as suitable for ion implant annealing, and as expected were found to introduce no problems due to type conversion. As a further precaution a simple electrical breakdown check was carried out on the wafer surface after mesa etching to ensure that the conducting layers had been removed.

The second successful area of process monitoring was the use of a Dektak IIA surface profiler to measure etch depths in the presence of photoresist masks. This technique was employed during the first mesa etch and the subsequent N^+ ohmic contact etch.

Finally the incorporation of a drop in ohmic test pattern (photograph 9) demonstrated that the higher than expected series resistance of the diode was not due to the contact technology. However it has subsequently been concluded that future test patterns should be made more representative of device areas. For example a test pattern comprising a single finger and cut out pad incorporated into the ohmic metallisation mask would have allowed a more accurate determination of the series resistance contribution of the epi layers. Measurements on a range of simple pad configurations would also assist in determining more precise models for assessing future device layouts.

With regard to the overall layout philosophy, it is now clear that the 5 micron alignment tolerance could be reduced considerably. In practice patterns were consistently aligned to within 1 micron (see photograph 8), and even after prolonged etching the mesa edges did not undercut by more than 2 microns. It is suggested that the alignment tolerance could be reduced to 3 microns without comprising the yield.

The dielectric "doormat" technology proved successful and reliable and will allow future devices of an N on N^+ configuration to be made. It is worth noting that wafer D which incorporated plating of the circuit tracks inadvertently included an air bridge rather than a "doormat" under each of the fingers. The O_2 ash required to remove the plating mask also removed the polyimide doormat (photographs 10 and 11). This technique, perhaps using baked photoresist rather than polyimide, is well worth further investigation. A further implication of photographs 10 and 11 is that the technique used to incorporate plating into the processing schedule is not compatible with the preceeding technology. Only the final wafer, D, had this step incorporated into the process scheme and therefore no attempt was made to overcome this problem. The use of a silicon nitride passivation layer could possibly provide a satisfactory solution.

7. Conclusions

In order to satisfactorily complete the fabrication of this varactor based MMIC, it was necessary to implement a process schedule incorporating seven separate photolithographic masking stages and more than 40 discrete process steps. This scheme is more complex than any previously tackled in DP2, and in overall complexity is comparable to the schemes used in the more usual FET based MMIC fabrication processes. The successful realisation of these components can be attributed to the conservative design rules employed and the careful use of process monitoring throughout the scheme.

Components from this work have been used by DP1 in their subsystem research, and the results from these studies will be reported at a later date. In addition the process scheme has ncw been transferred to an external contractor who has used it largely unchanged to provide greater quantities of prototype components for the DP1 research. The successful transfer of this process is a further measure of the confidence established in the approach selected to satisfy this requirement.

8. Acknowledgements

9. References

1. S M Sze, "Physics of Semiconductor Devices, 2nd Ed. publ. by Wiley-Interscience, 1981, p 101.

2. D J Taylor and K P Hilton, "Contact resistance measurements to Ge:Au and Ge:Au:Ni ohmic contacts to N type GaAs", ME2 Research Note No 17, 31st July 1985.

3. L B Ta, H M Hobgood, A Rohatgi, and R N Thomas, J. Appl. Phys. 53(8), 5771 (1982).

Appendix A

POLYIMIDE PATTERNING

The patterning technique adopted relied on covering the whole of the wafer with polyimide and subsequently plasma ashing using a metal mask to protect the wanted regions of the polyimide. After ashing the metal mask can be removed leaving the required pads of polyimide.

The polyimide used for the investigation was NOLIMID 32 which was spun on at 6000 r.p.m. and cured in a vacuum oven using the following schedule:-

Ramp oven up to $260^{\circ}C$, at 3 C./min.
Hold at $260^{\circ}C$. for 1 hour.
Allow to cool naturally to ambient (approx. 3 hours).

A 1000 A thick titanium layer was used for the protection layer during ashing. This can be removed with a short (5 min.) etch in dilute HF (1 part HF to 500 parts H_2O).

A test mask (DP2 electron beam lithography file no. TSIPI.M2) was made up which consisted of a comb structure where the sizes of the fingers and gaps progressively increased in 5 micron steps from a minimum of 5 micron finger/5 micron gap up to 25 micron finger/25 micron gap (photograph 12). This pattern was exposed using standard electron lithography techniques followed by a standard Ti metallising and float off.

The nature of this mask allows a very clear determination of undercut to be made i.e. if the 5 micron finger vanishes then undercuts of > 2.5 microns are implied. The sizes of the remaining fingers and gaps allow a more accurate estimate to be made.

Several samples were prepared as described above and a series of experiments using the standard barrel asher conditions (50 W incident R.F power with an O_2 flow of 150 cc/min giving a working pressure of 2 Torr) were carried out. The best results achieved were undercuts of between 2 and 3 microns after 55 mins ashing, photograph 13.

A second set of experiments were carried out with the wafer mounted vertically along the axis of the asher, all other conditions as before. Although the undercut was approx. 5 microns after 20 mins. the ashing seemed more even across the slice and the edges of the polyimide pads looked better defined (photograph 14).

A third set of experiments were carried out with the slice vertical at a reduced O_2 flow of 20 cc/min giving a working pressure of 300 mtorr. This gave consistent results with undercuts of 1 micron or less after 40 mins. ashing. The unwanted polyimide was fully removed from the unprotected areas (photograph 15). The holes etched in the body of the pad apparent in photograph 15 were due to pin holes in the Ti ashing mask. By increasing the Ti thickness to 2000 A this problem was eliminated. These conditions were subsequently used in

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the fabrication of the varactor diodes described in this note.

SUMMARY

NOLIMID 32 polyimide, spun at 6000 r.p.m.
SLOW CURE, 3 C/min. to 260 C then hold at 260 C for 1 hour.
MASK, 2000 A of titanium
ASH, 50 W incident power, 20 cc/min O_2 flow, slice vertical, 300 mtorr pressure.

Appendix B

CAPACITORS

The recommended full polyimide curing cycle includes a bake at 400°C. Past experience has shown that this is incompatible with ohmic or Schottky contacts already fabricated on the wafer. Therefore a cure cycle based on a maximum temperature of 300°C is used. [The full cure cycle is described in Appendix A].

A photolithography mask set was available which defined capacitors with areas between 3×10^{-4} cm^2 and 2×10^{-5} cm^2 (photograph 16). The processing schedule for this mask set is outlined below.

1) Pattern, metallise and float off the bottom capacitor plate and contact pad.

2) Spin and cure the polyimide.

3) Pattern, metallise and float off the polyimide patterning mask.

4) O_2 ash polyimide to form required patterns.

5) Remove patterning mask.

6) Pattern, metallise and float off the top capacitor plate and contact pad.

Completed wafers were measured on an autoprober, and a typical histogram for the largest area capacitor is shown in figure 14.

The results for a typical wafer are shown in figure 15 where the measured capacity is plotted against the length of the side of the square pad forming the capacitor plate. All 3 wafers measured showed the marked turn over below 0.1 pf and this was assumed to be due to residual strays of approximately 0.07 pf. If these strays are assumed to be constant and are subtracted from all the readings, then an assumed dielectric constant of 4.55 for the polyimide gives the agreement between theoretical and practical results shown in figure 16 where the standard deviation corresponds to a tolerance of between $\pm$ 3% for the largest pads and $\pm$ 6% for the smallest.

The average yield of capacitors was consistently better than 70% with the majority of failures located around the perimeter of the wafers. Yields of 96% were obtained if the edge patterns were not included in the measurements.

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Appendix C

DETAILED DESCRIPTION OF THE PHOTO-LITHOGRAPHIC MASKS

Each mask will be described separately with its function and any special features explained. Details of the overall microwave circuit have been omitted from the drawings.

The masks were made of low reflectivity chromium deposited on Crown glass plates 3 inches square and 0.060 inch thick. Each device is 10 mm x 8 mm and the 4 x 5 array has an overall size of 40 x 40 mm.

Mask 1

Most of the N on N^+ layer must be etched away to expose the semi-insulating GaAs. This mask defines small islands or mesas of N on N^+ which will remain to form varactor diodes. Similar mesas are required at a later stage for checking the quality of ohmic contacts.

Registration

Pairs of small squares, 4 pairs for each device, produce mesas which allow registration of subsequent masks. The left hand one of each pair is used to align Mask 2 and the right hand one locates Mask 3.

Registers

Registers

Mesa for
Varactor

MASK 1

Register for
mask 3

Mesa for
Ohmic Contact
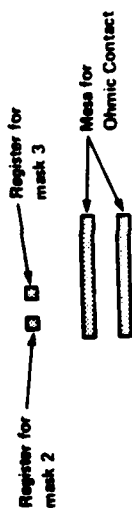
Register for
mask 2

Registers

Mask 2

This mask defines where the N layer will be etched away to expose the N^+ layer to allow subsequent ohmic contacting. Narrow fingers of N are left for the Schottky contact metallisation on the varactor. The transmission line ohmic test pattern will be formed on rectangular bars of N^+.

Registration

Most of the mask is opaque, small clear registration squares allow alignment with similar smaller mesa squares etched on the wafer during step 1. Mesa squares which will be used for alignment of Mask 3 are protected from the etch by photo-resist.
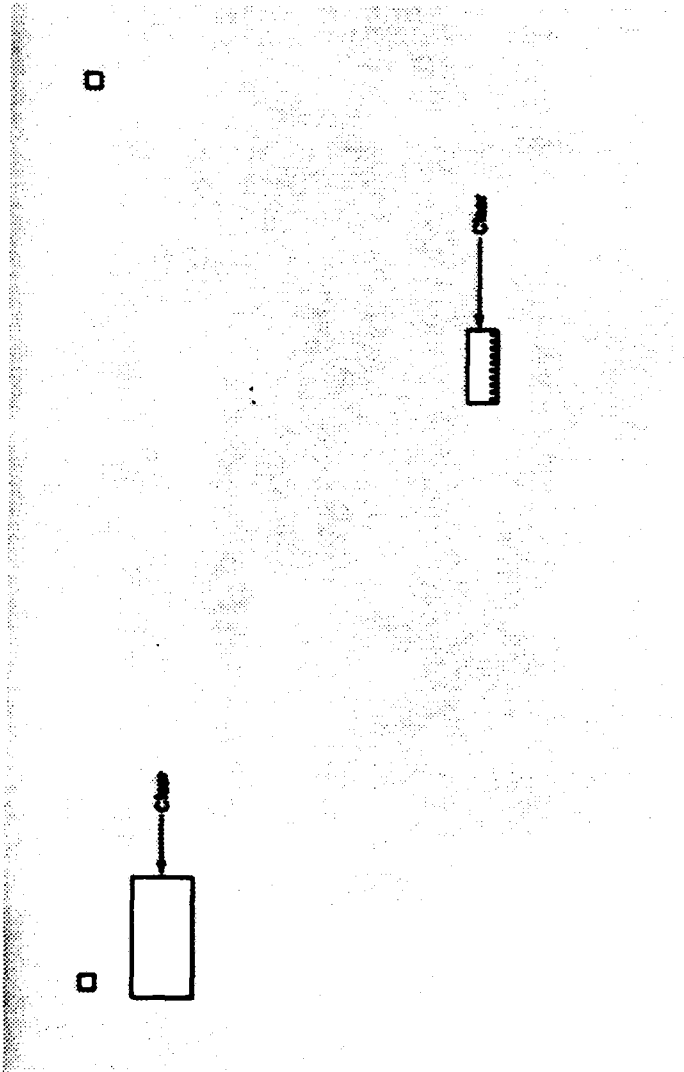
MASK 2

Mask 3

The mask defines the microwave circuit and ohmic contacts for the varactor. The ohmic test pattern is also metallised. In addition connections are made to the circuit to allow gold plating at a later stage. (See photographs 2 and 16 showing metallised ohmic contact and narrow fingers of N material for the Schottky contact).

Registration

Four groups of 12 squares on each pattern are formed to allow alignment of the next masks. (Refer to photograph 9).

Clear

MASK 3
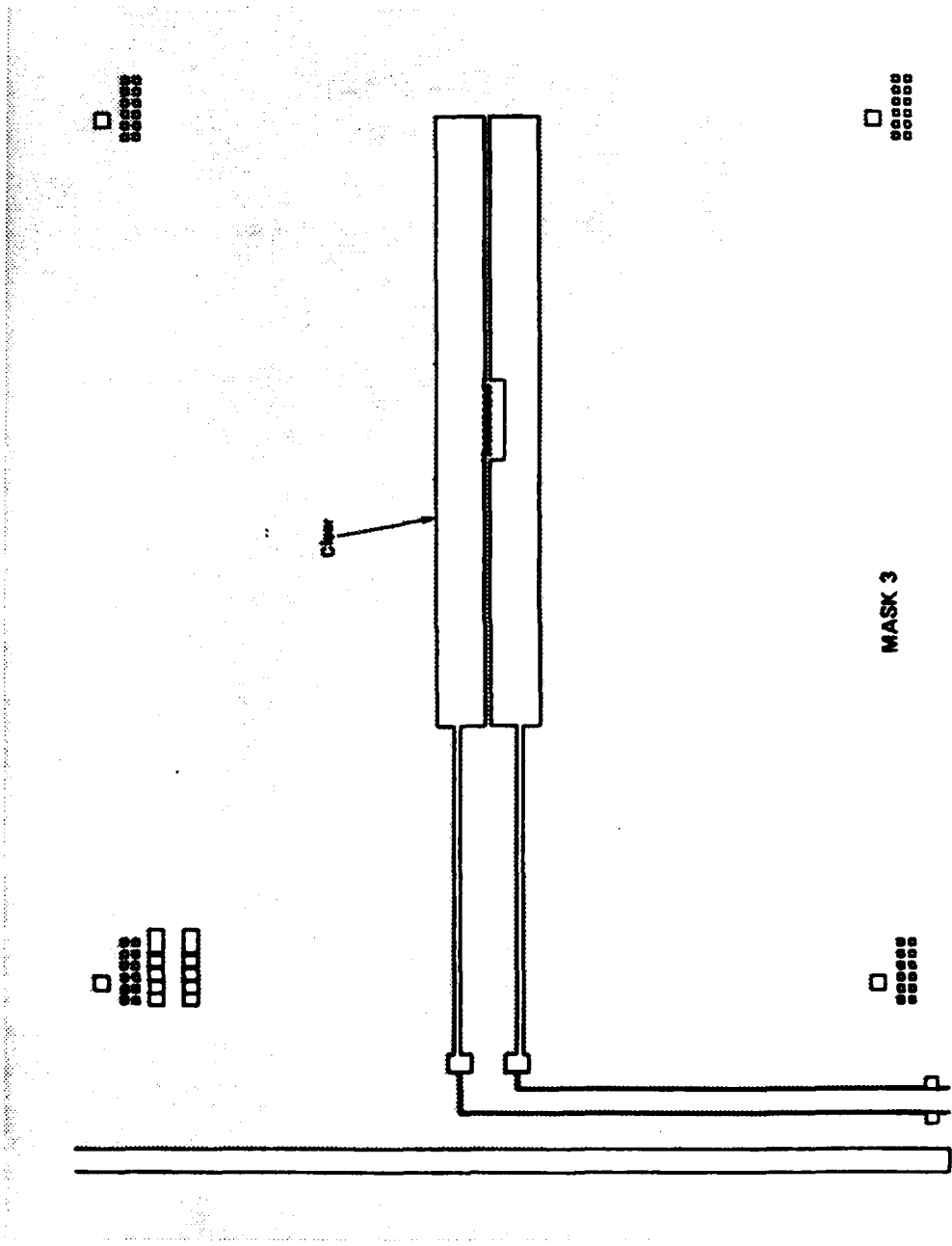
Mask 4

The mask is used to pattern the polyimide dielectric film which is used as an insulator on the varactor and the fixed capacitors. See appendix A for details of polyimide patterning.

Registration

A clear square in the mask just fits over 4 gold squares in the 12 square pattern on the wafer. (See photograph 9).

MASK 4
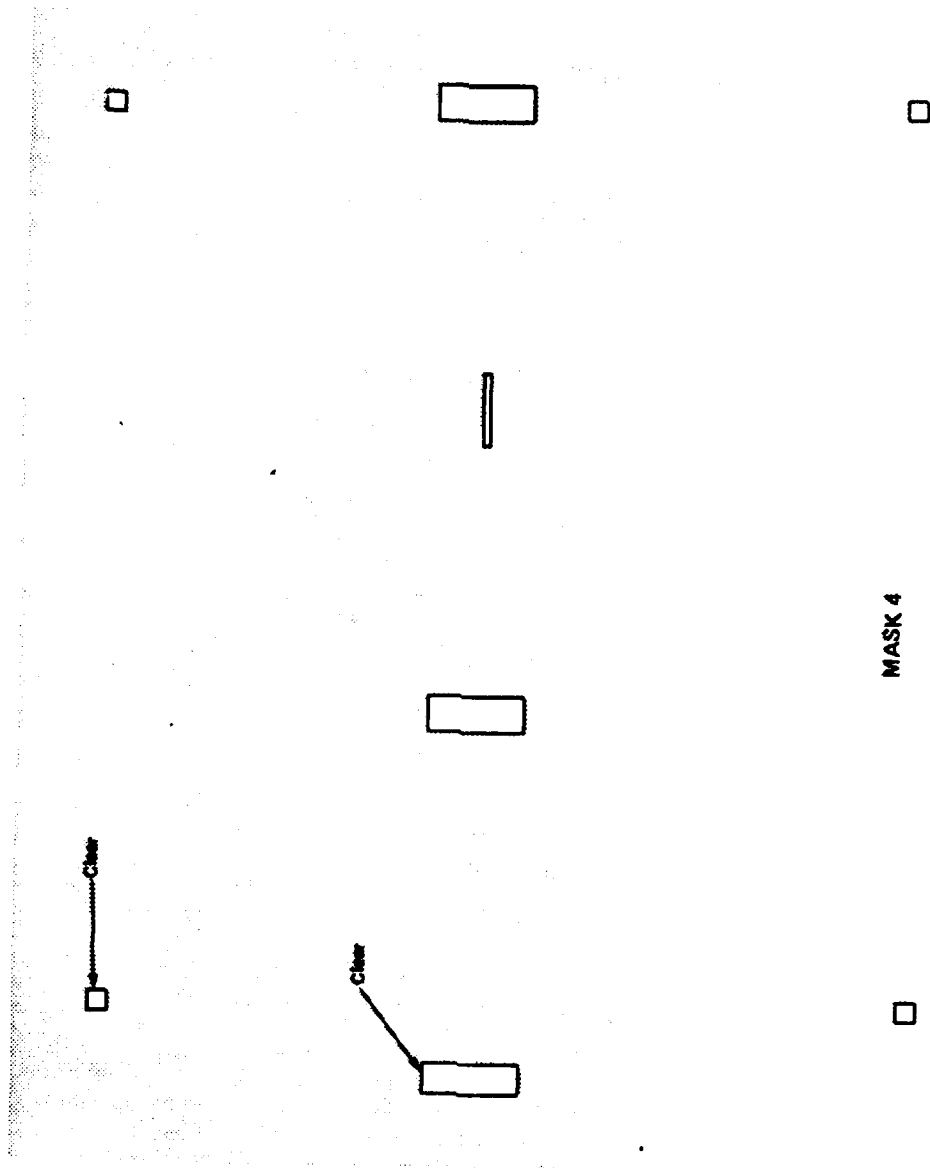
Clear

Clear

Mask 5

This mask is used to define the Schottky contact on the varactor diode and provides the top plates for the fixed capacitors. (See photographs 1 and 4 for the varactor, and photograph 3 for the capacitor).

Registration

A clear square in the mask just fits over the centre 4 gold squares in the 12 square pattern of gold on the wafer. There are 4 registrations for each device. (See photograph 9).
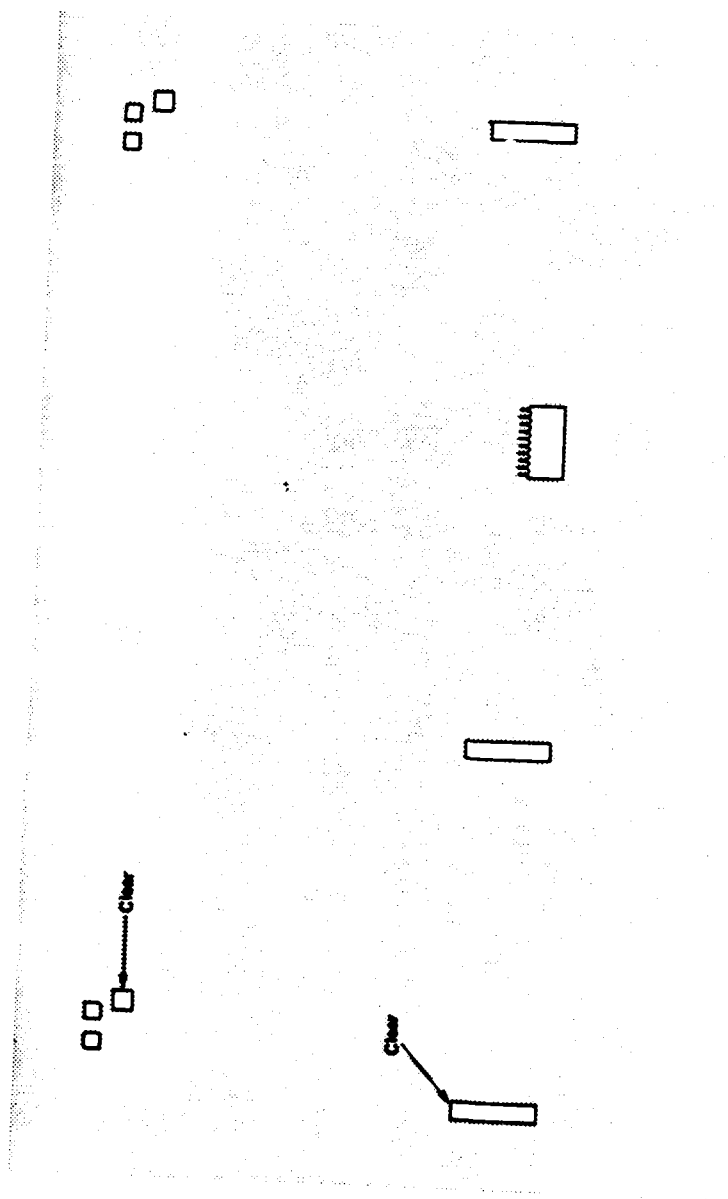
MASK 5

Clear

Clear

<u>Mask 6</u>

This mask defines areas to be gold plated. Photo-resist prevents plating where it is not required.

<u>Registration</u>

A clear square on the mask fits over the right hand set of 4 gold squares in the 12 square pattern on the wafer. There are 4 alignment squares for each device. (See photograph 9).

Clear

Clear
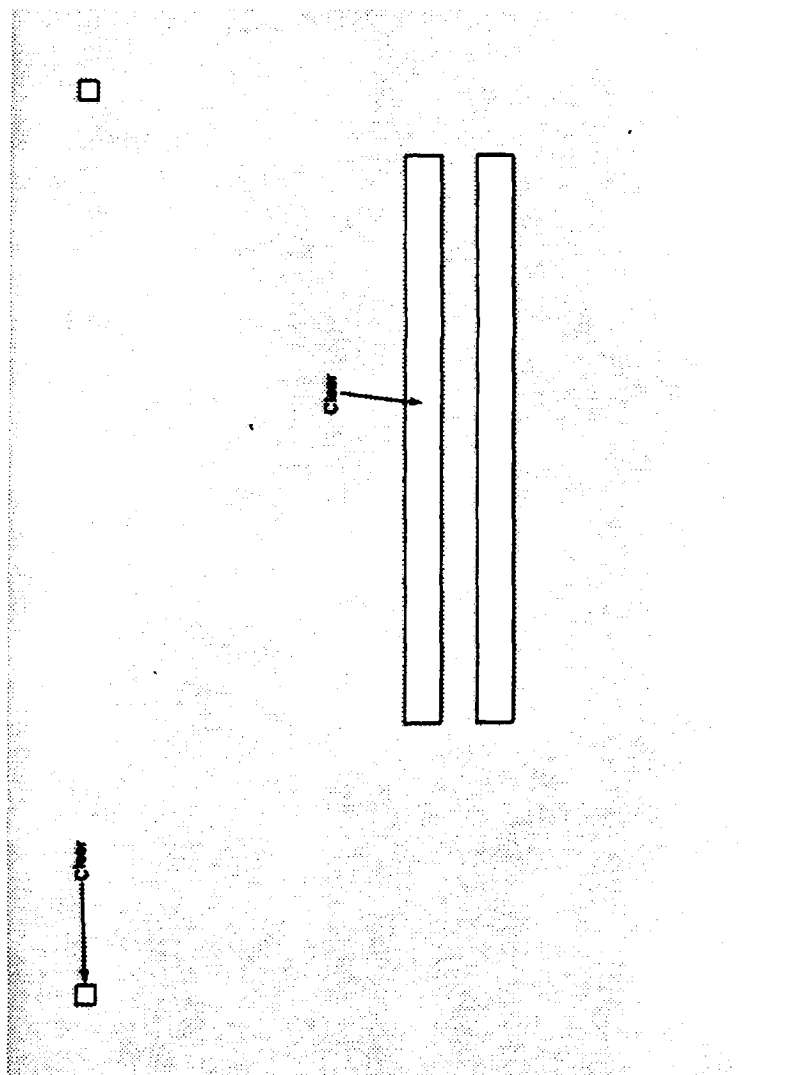
MASK 6

Mask 7

This mask allows the gold plating ties to be removed by etching. Photo-resist protects all other regions. In practice this mask was not used as the metal plating ties were cut through and isolated during the dicing stage.

Registration

Clear squares in the mask allow alignment with the same set of gold squares on the wafer used to align Mask 6.

MASK 7
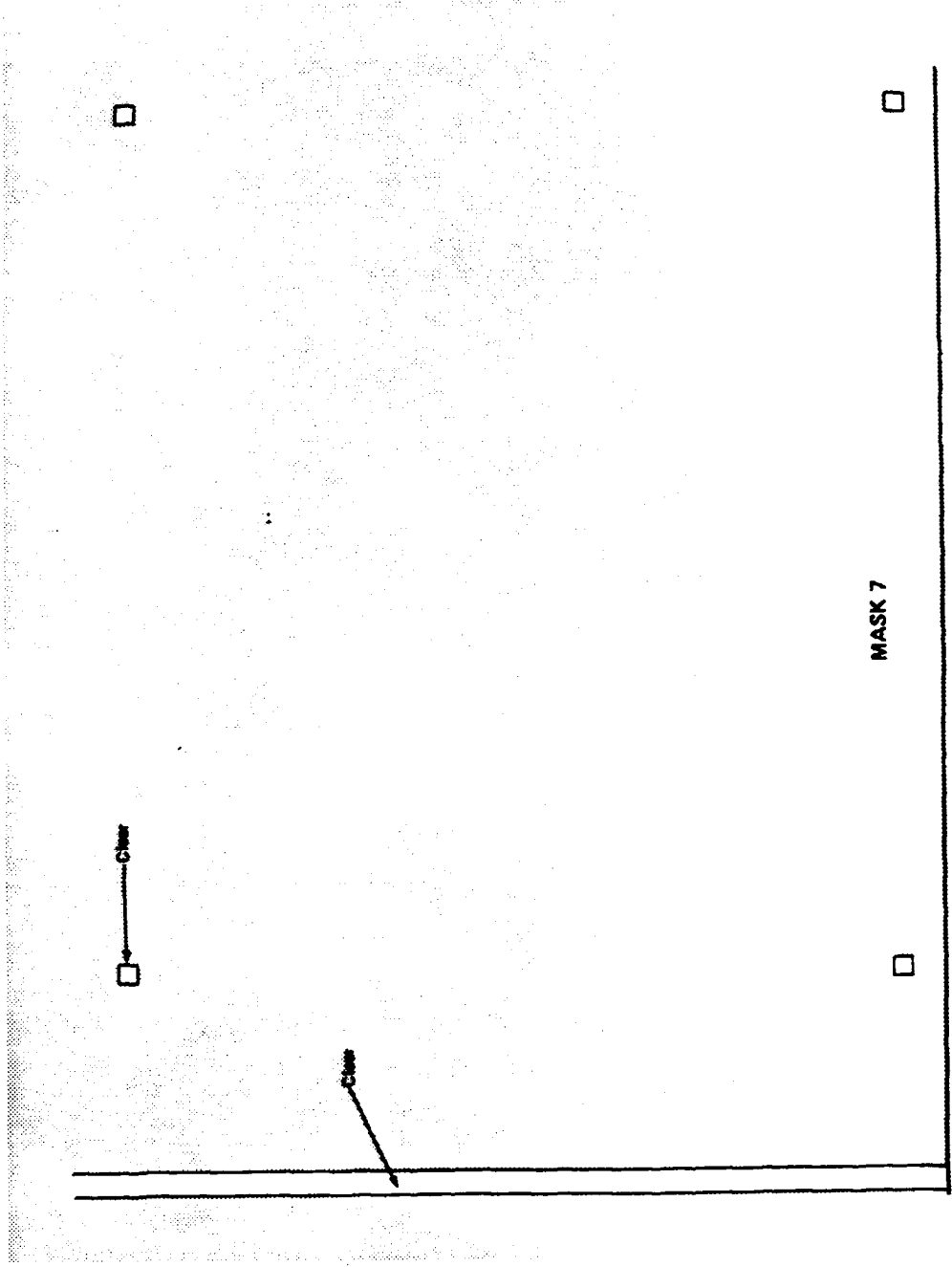
Appendix D

DETAILED PROCESS SCHEDULE

      R.S.R.E.   ME2 Div.   N on N^+ Varactor process   B.T.H & J.T.P

      PROCESS DETAILS FOR VARACTOR TYPE 1 (PLATED VERSION)
      ****

1)   CLEAN SLICE
2)   SPIN PHOTO RESIST

***** 3)   EXPOSE MASK 1 ***** (TO ETCH THROUGH N & N^+ DOWN TO S.I.)

4)   PRE ETCH BAKE
4a) PHOTOGRAPH WAFER USING PHASE CONTRAST (Mag X13)
4b) MEASURE PHOTORESIST USING DEKTAK
5)   ETCH DOWN TO SEMI INSULATING (THROUGH N AND N^+ LAYERS ** CHECK
THIS **)
6)   ASH RESIST OFF SLICE
6a) MEASURE ETCH STEP (DEKTAK)
7)   SPIN PHOTO RESIST

***** 8)   EXPOSE MASK 2 ***** (TO ETCH THROUGH N LAYER DOWN TO N^+)

9)   PRE ETCH BAKE
10)   ETCH THROUGH N LAYER JUST INTO N^+ LAYER
10a) EXAMINE USING PHASE CONTRAST (Mag X161)
10b) MEASURE PHOTORESIST THICKNESS (DEKTAK ACROSS FINGERS)
10c) MEASURE ETCH STEP RELATIVE TO TOP OF PHOTORESIST (USE DEKTAK)
11)   ASH RESIST OFF SLICE
11a) MEASURE ETCH STEP USING DEKTAK
12)   SPIN PHOTO RESIST, CHLOROBENZENE PROCESS

***** 13) EXPOSE MASK 3 ***** (OHMICS & FIRST LEVEL METAL, INCLUDING
TIES)

******* CARRY OUT 14 to 17 IN ONE WORKING DAY *******

14)   10% AMMONIA DIP
15)   OHMIC METALLISATION (200 A OF Ge,, 500 A of Au, 3000 A of top up
Au)
16)   FLOAT OFF
17)   ALLOY OHMICS
17a) PHOTOGRAPH OHMIC METAL (X13 & X160)
17b) MEASURE OHMIC THICKNESS (DEKTAK)
18)   COAT WITH POLYIMIDE
19)   CURE POLYIMIDE
20)   THIN POLYIMIDE, STANDARD HORIZONTAL ASH FOR 30 mins.
21)   SPIN PHOTO RESIST, CHLOROBENZENE PROCESS

***** 22) EXPOSE MASK 4 ***** (TITANIUM ASHING MASK)

23)   TITANIUM METALLISE, 2000/4000 A, FLOAT OFF

24) PATTERN POLYIMIDE, 0.4 torr, 50 W, SLICE VERTICAL, approx. 2/3 hrs
25) REMOVE TITANIUM, DILUTE HF, approx 30 mins
25a) PHOTOGRAPH POLYIMIDE (X13 & 160)
25b) MEASURE POLYIMIDE THICKNESS (DEKTAK)
26) SPIN PHOTO RESIST, CHLOROBENZENE PROCESS

***** 27) EXPOSE MASK 5 ***** (SCHOTTKY & SECOND LEVEL METAL)

27a) PHOTOGRAPH PHOTORESIST PATTERN BEFORE METALLISATION (X160 & X798
28) SCHOTTKY METALLISATION, 1000 A Ti, 1000 A Pd, 1000 A Au, 2000 A top up Au
29) FLOAT OFF
29a) PHOTOGRAPH FLOATED OFF AREAS (X32 & X160)
29b) DEKTAK OVER CAPACITOR, MEASURE POLYIMIDE AND TOP METAL THICKNESS

***** 30) EXPOSE MASK 6 ***** (PLATING MASK)

31) BAKE PHOTORESIST PRIOR TO PLATING
31a) USE DEKTAK TO ESTABLISH BASELINE
32) PLATE WITH GOLD (3 microns?)
32a) USE DEKTAK TO CHECK GOLD THICKNESS AND REPEAT 32) IF REQUIRED
33) REMOVE PHOTORESIST
34) CHECK GOLD THICKNESS (DEKTAK)
35) SAW INTO DICE

Appendix E

GOLD PLATING

The Engelhard E-59 Industrial Process was used. Special jigs were made to hold 2 inch wafers. The jig design will allow plating on both faces of the wafer. The thickness of plated gold can be directly measured using the Dektak or it can be calculated from the weight of gold deposited provided the plated area is known.

The basic details are given below.

ENGELHARD E-59 INDUSTRIAL GOLD PROCESS
PLATINUM ELECTRODES
VOLUME OF BATH   1.4 Litres
CURRENT DENSITY 2 to 5 mA/sq. cm.
PLATING RATE AT 65°C, 0.11 micron per min at 2 mA/sq. cm.

OHMIC CONTACT

N⁺ GaAs
2×10^{18} cm^{-3}

0.2 microns

Schottky Contact

N GaAs
1×10^{17} cm^{-3}

0.3 microns

Semi Insulating GaAs Substrate
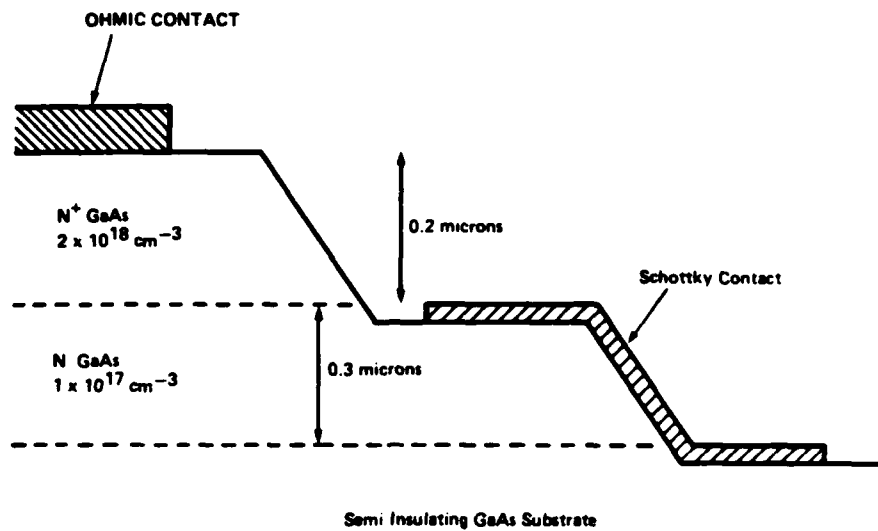
FIG 1   FET TYPE MATERIAL STRUCTURE

Schottky Contact

N GaAs
1×10^{17} cm^{-3}

0.5 microns

Ohmic Contact

N⁺ GaAs
2×10^{18} cm^{-3}

2 microns

Semi—Insulating GaAs Substrate
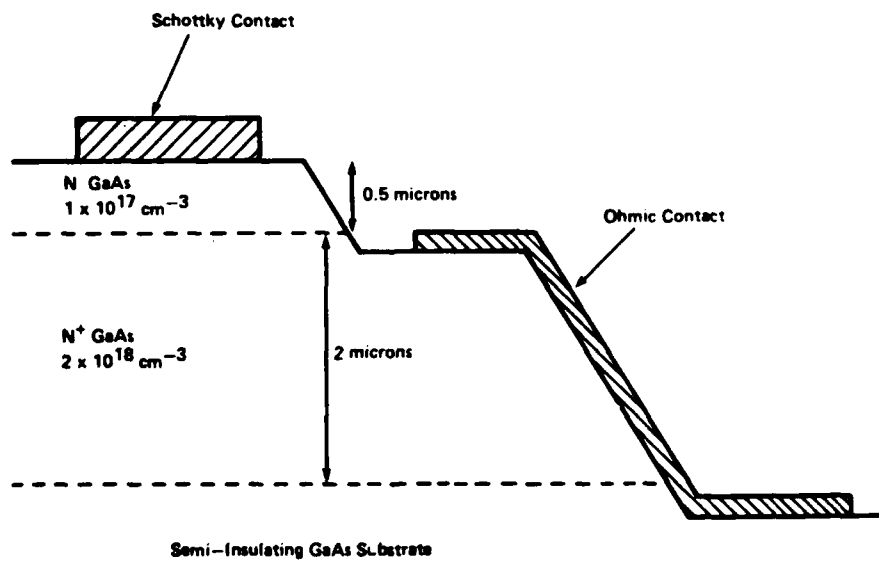
FIG 2   VARACTOR DIODE MATERIAL STRUCTURE

898 ('n' type)
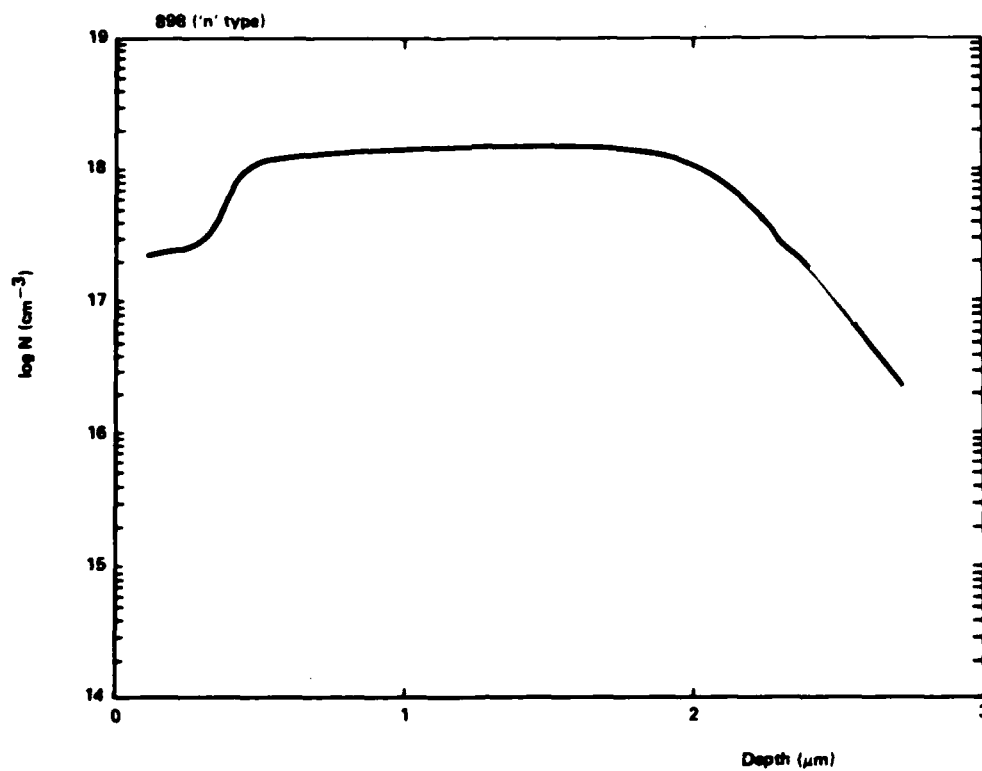
FIG 3 POST OFFICE PROFILER PLOT OF VARACTOR LAYER
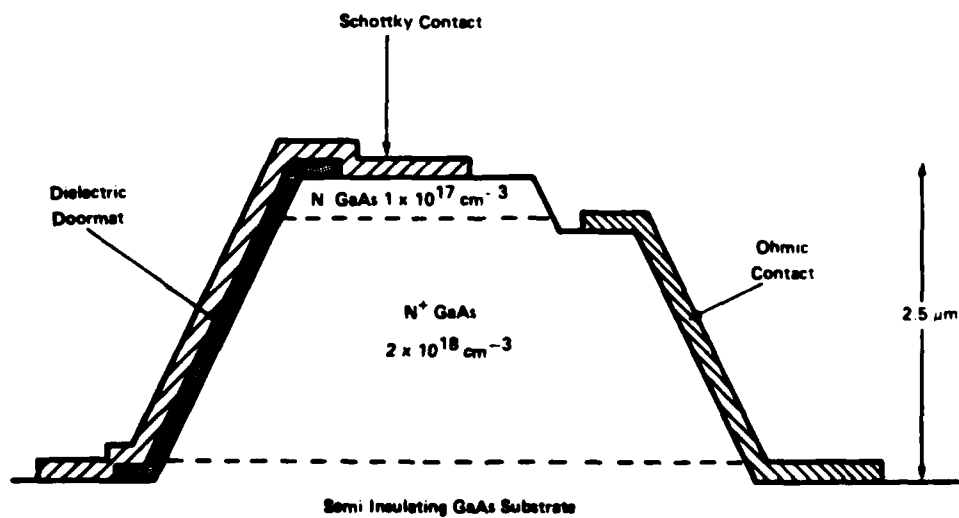
FIG 4   DIELECTRIC "DOORMAT"
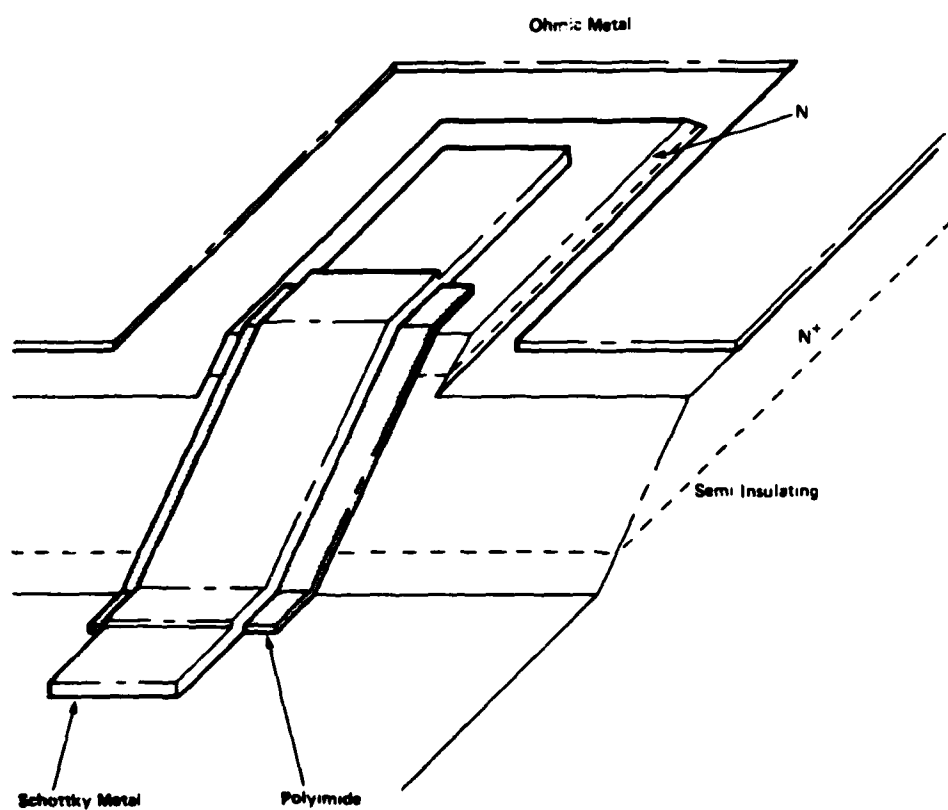
FIG 5   DETAIL OF DIODE GEOMETRY
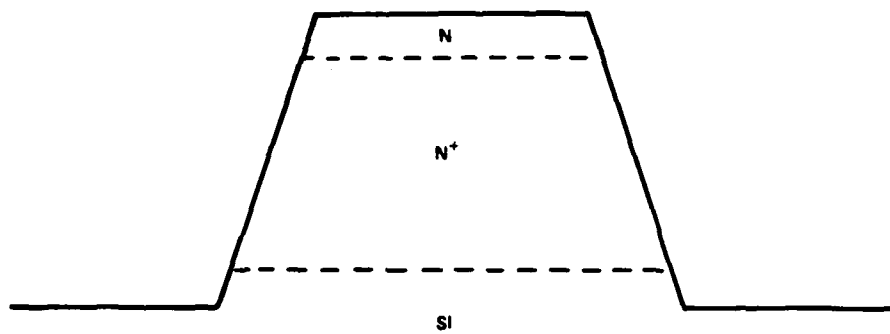
FIG 6   FIRST MESA ETCH
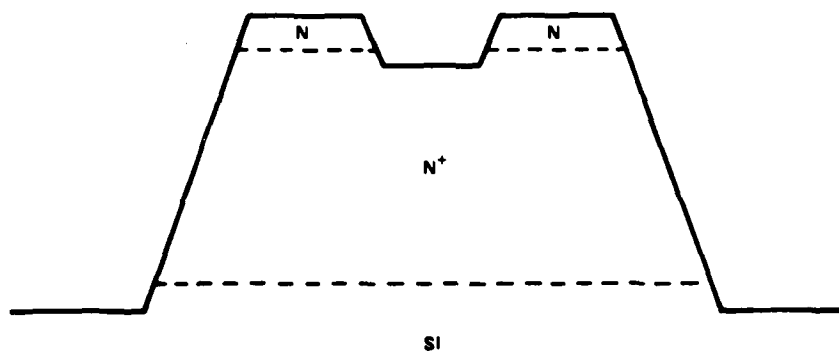
FIG 7   ETCH FOR OHMIC CONTACTS
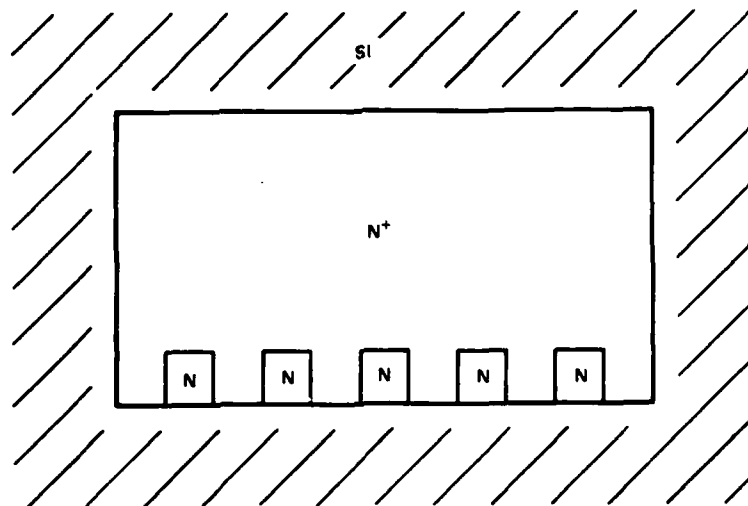
FIG 8   DIODE MESA AFTER ETCHING STAGES
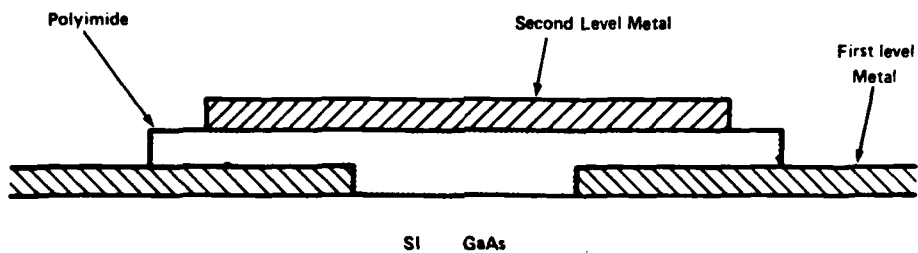
FIG 9   CAPACITOR CONSTRUCTION

AREA 2500 SQ MICRONS NO EXTERNAL CAPS VAR1Bb
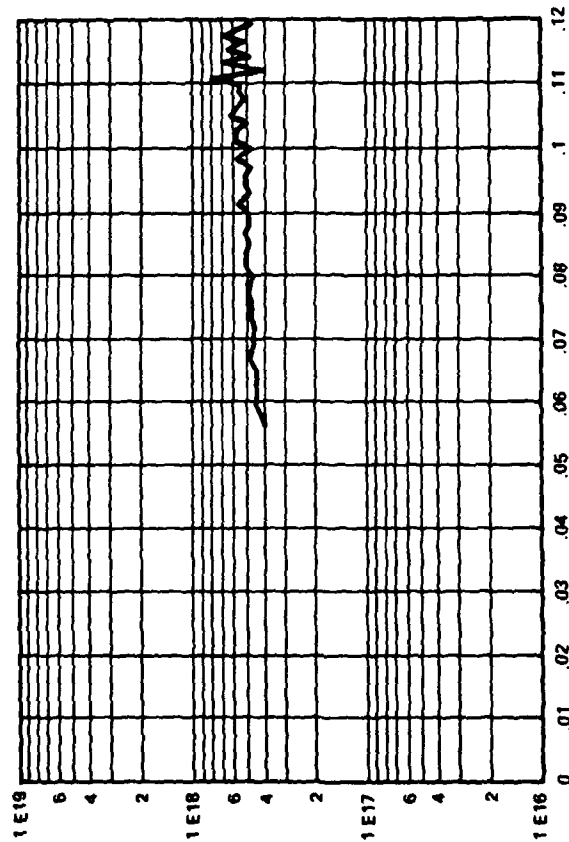
V1 BBP
Nd PROFILE

Nd/cc
Plotted against
Depth (Microns)

ETCH:– 0 uM

FREQUENCY:– 1 MHz
AREA:– 2.5E–5

* –DP2 DIVISION – *
* –RSRE MALVERN– *

FIG 10 PROFILE OF N LAYER ON WAFER B OBTAINED FROM C/V
MEASUREMENTS OF DEVICE b

VAR 1D No 1 ALL EXTRA CAPS REMOVED

VAR1D1P
Nd PROFILE

Nd/cc
Plotted against
Depth (Microns)

ETCH:– 0 uM

FREQUENCY:– 1 MHz
AREA:– 2. 5E –5

* – DP2 DIVISION – *
* – RSRE MALVERN ... *
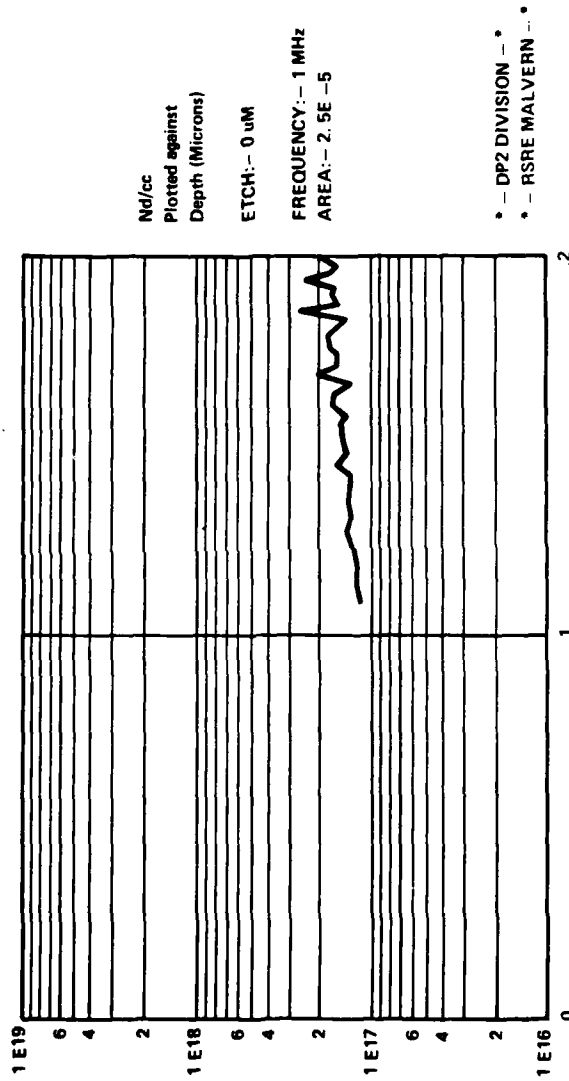
FIG 11   PROFILE OF N LAYER ON WAFER D, OBTAINED FROM C/V
MEASUREMENTS ON DEVICE 1

VAR1D No 5 ALL CAPS REMOVED 2500 SQ UM AREA

VAR1D5P
Nd PROFILE

Nd/cc
Plotted against
Depth (Microns)

ETCH:- 0 uM

FREQUENCY:- 1 MHz
AREA:- 2.5E-5

--DP2 DIVISION--
--RSRE MALVERN--
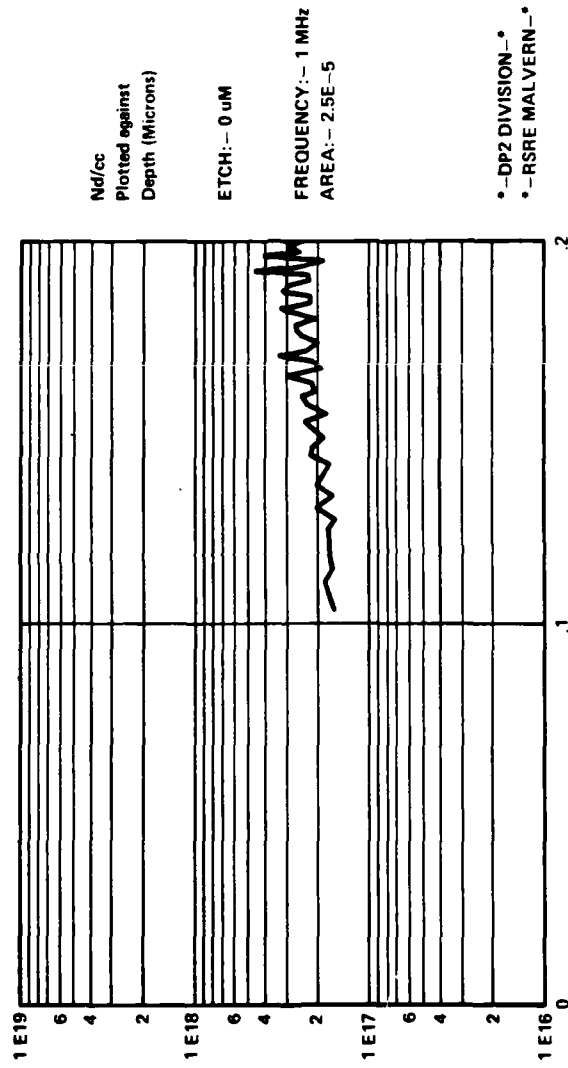
FIG 12   PROFILE OF N LAYER ON WAFER D, OBTAINED FROM
         C/V MEASUREMENTS ON DEVICE 5

AREA 2500 SQ MICRONS NO EXTERNAL CAPS VAR1Bb

Calculated

● $N_D = 4 \ 10^{17} \ cm^{-3}$

✕ $N_D = 2.5 \times 10^{17} \ cm^{-3}$

V1BBP
CAP/VOLT PLOT

FREQUENCY = .1 MHz

● – DP2 DIVISION – *
● – RSRE MALVERN – ●

Measured

CAPACITANCE (pF)

VOLTAGE (V)
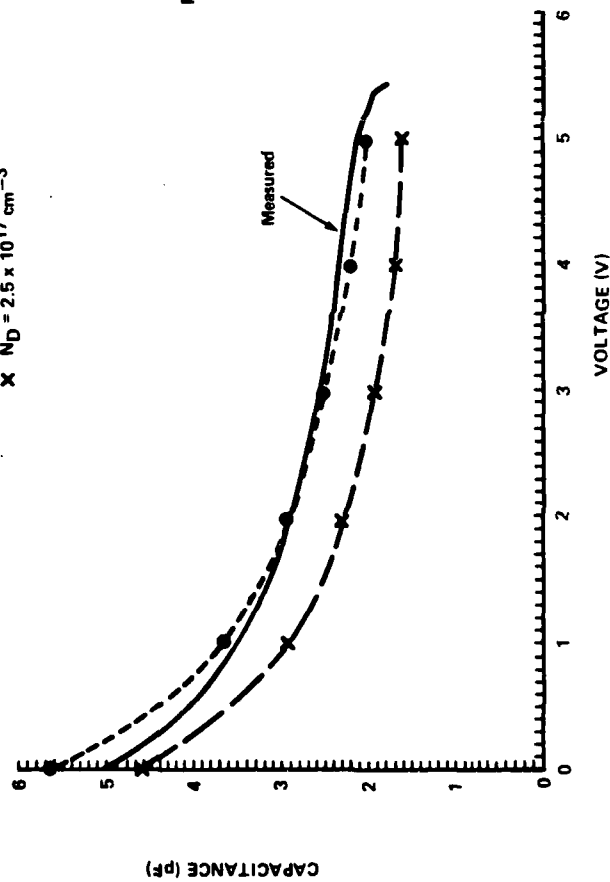
FIG 13   COMPARISON OF MEASURED AND CALCULATED
C/V CHARACTERISTICS ON WAFER B

CAP 3/1   BOX SIZE = .1 pF

TOTAL TESTED = 63   NUMBER DISPLAYED = 46   YIELD = 73%

            MEAN = 4 . 11   STD DEV = .24
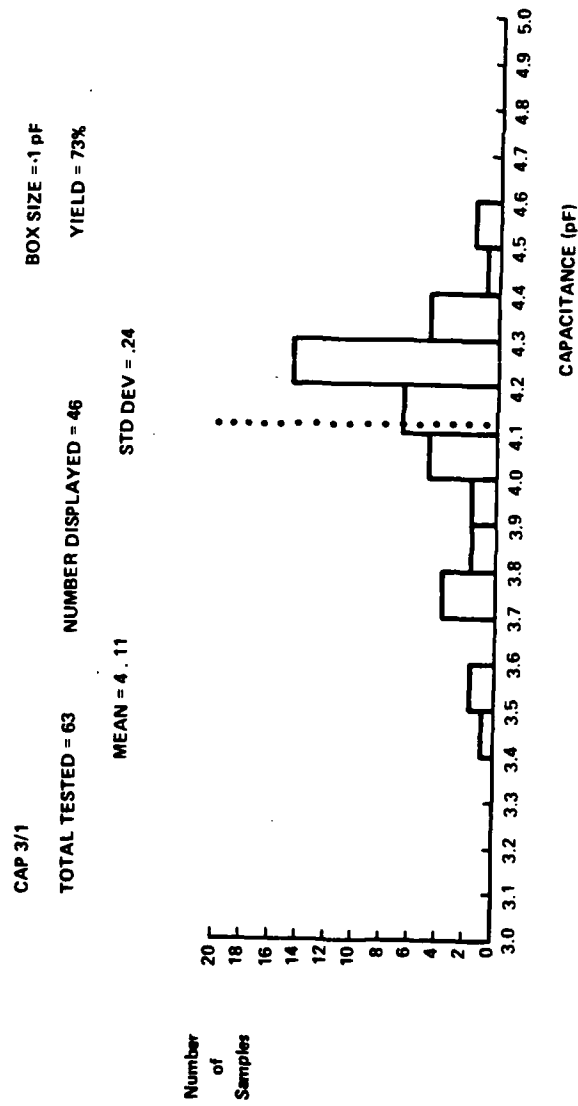
FIG 14   HISTOGRAM OF CAPACITANCE OF LARGEST AREA CAPACITOR

Wafer : CAP 3
Dielectric : ISOMID, 3 μm THICK
Sample size 60 devices of each value

Theoretical based on ϵ_{pI} = 3.5

⊙ measured value

Length
of side
of square
pad
(μm)

1000

100

10

.1

1.0

10.0

Capacitance (pF)

FIG 15   TYPICAL CAPACITOR TEST PATTERN RESULTS

Wafer: CAP 3

Dielectric: ISOMID, 3 μm THICK

Sample size 60 devices of each value

Theoretical based on $\epsilon_{PI} = 4.55$

△ measured value with .07 pF subtracted to allow for strays

Length of side of square pad (μm)
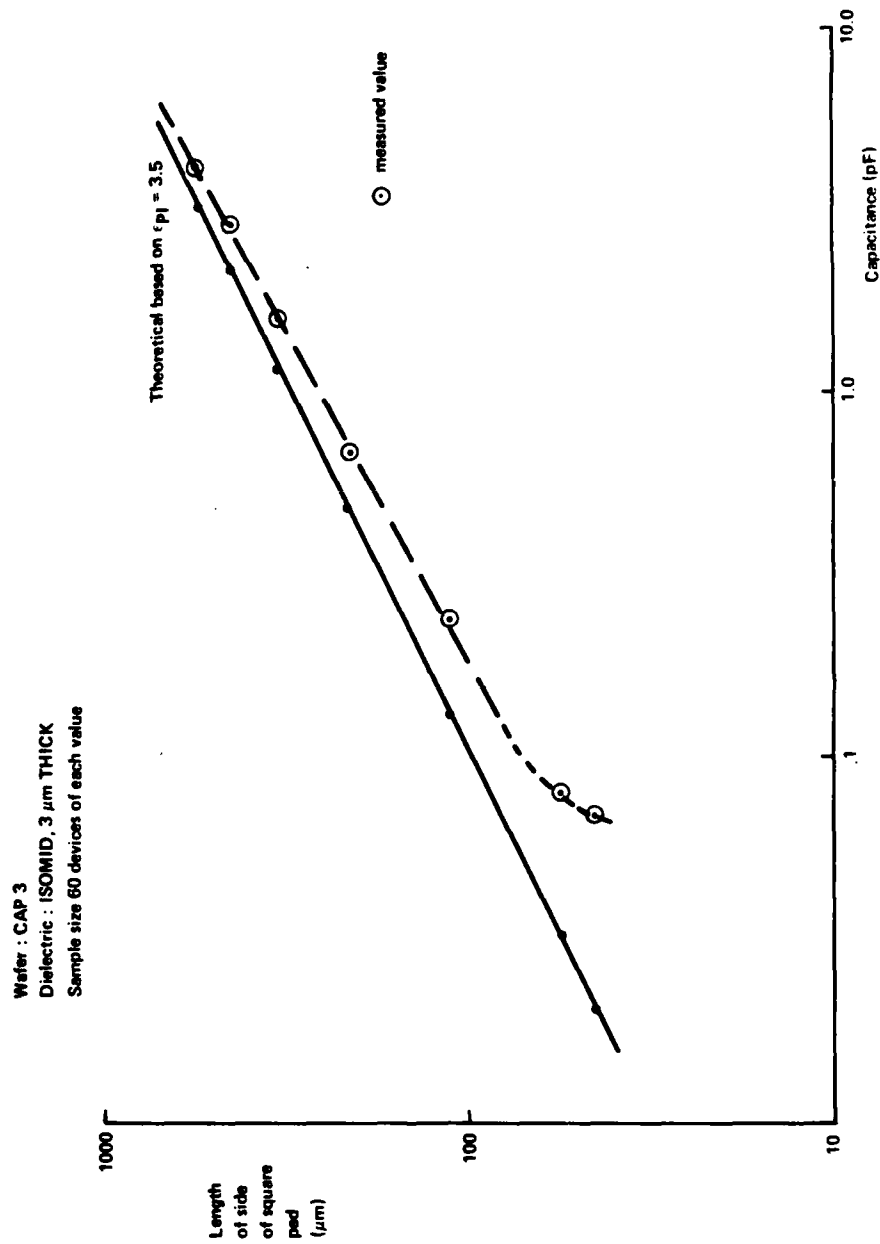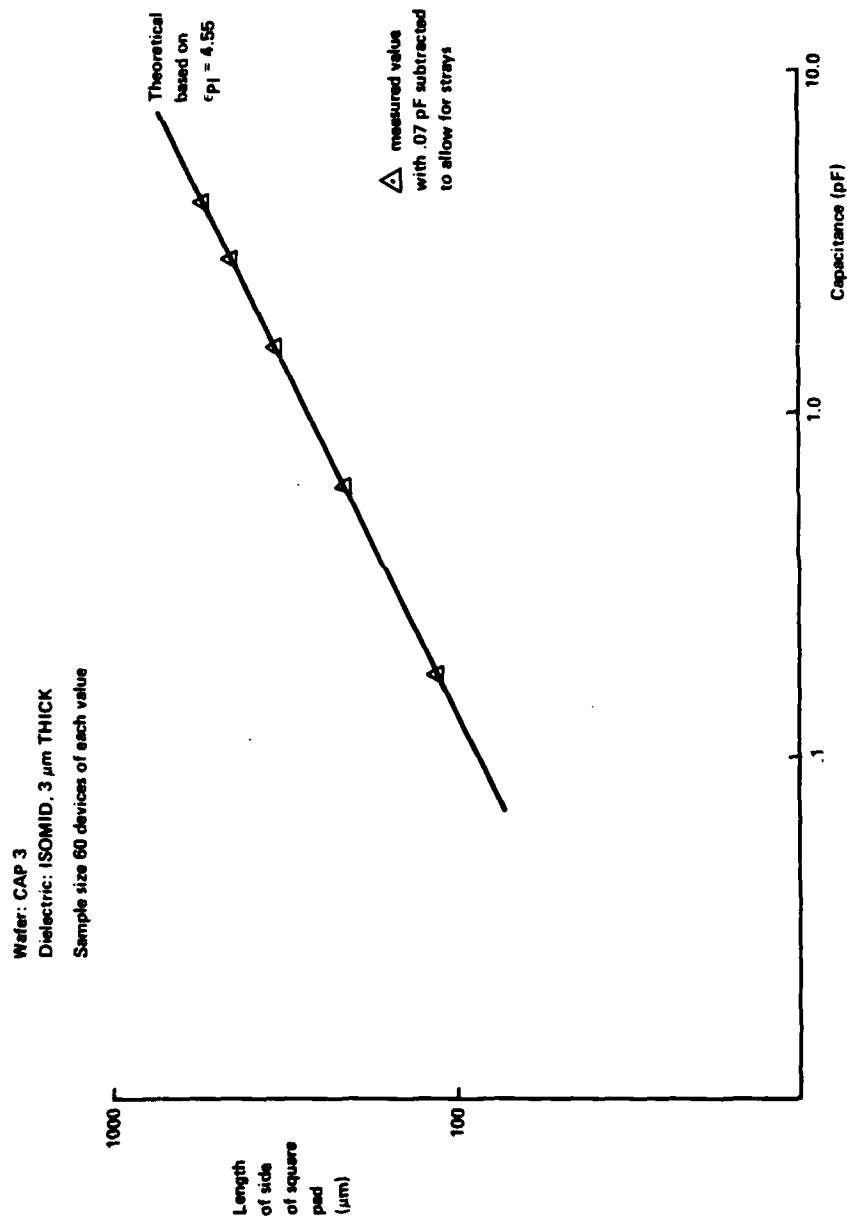
Capacitance (pF)

FIG 16   TYPICAL CAPACITOR TEST PATTERN RESULTS, MEASURED VALUES
ADJUSTED TO ALLOW FOR RESIDUAL STRAY CAPACITANCE
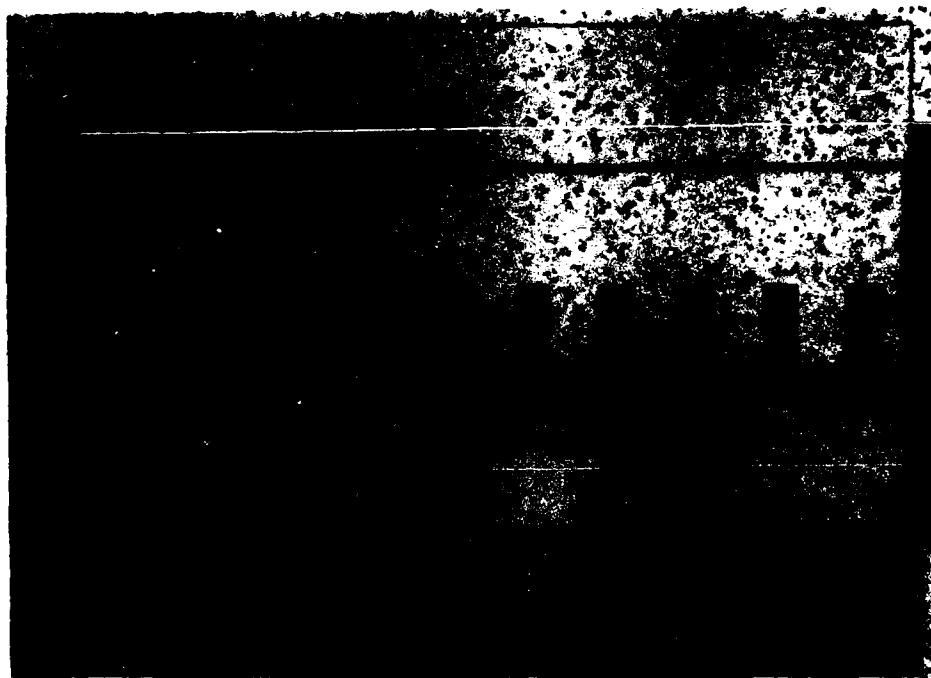
PHOTO 1   DIODE AREA
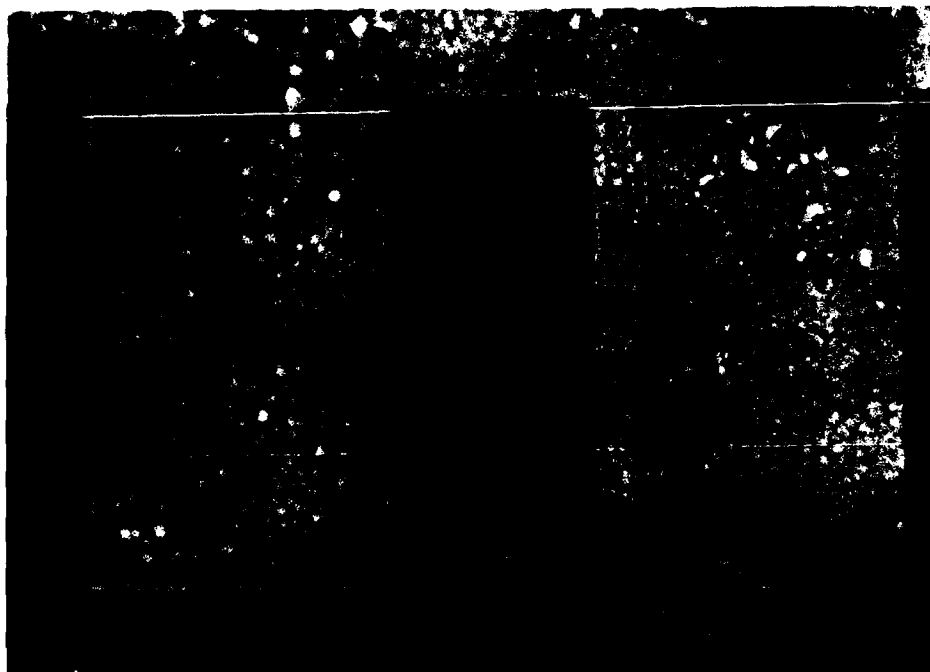
PHOTO 2 ALIGNMENT OF OHMIC CONTACTS AND MESAS
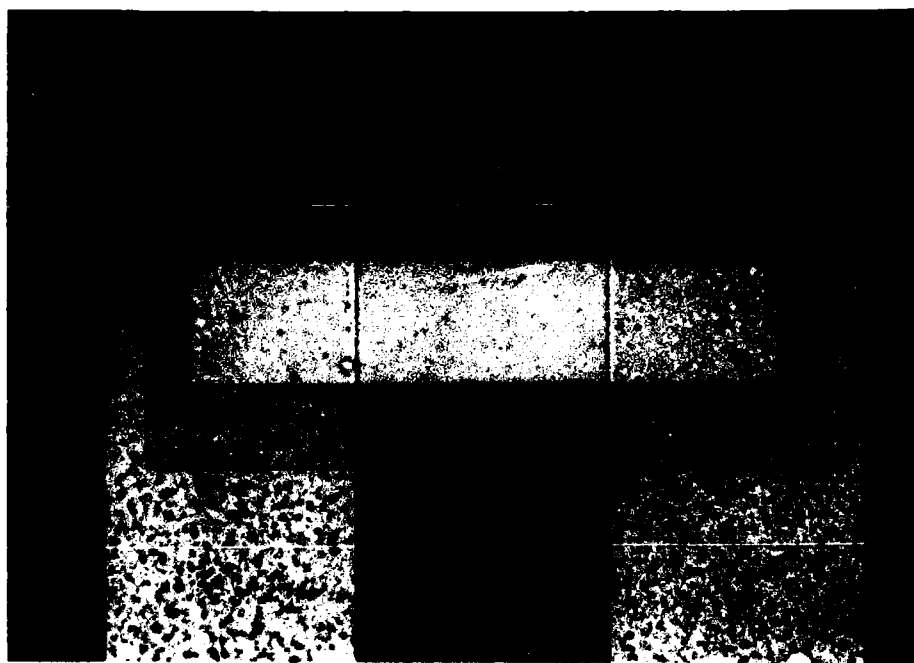
PHOTO 3   PLAN VIEW OF CAPACITOR PAIR
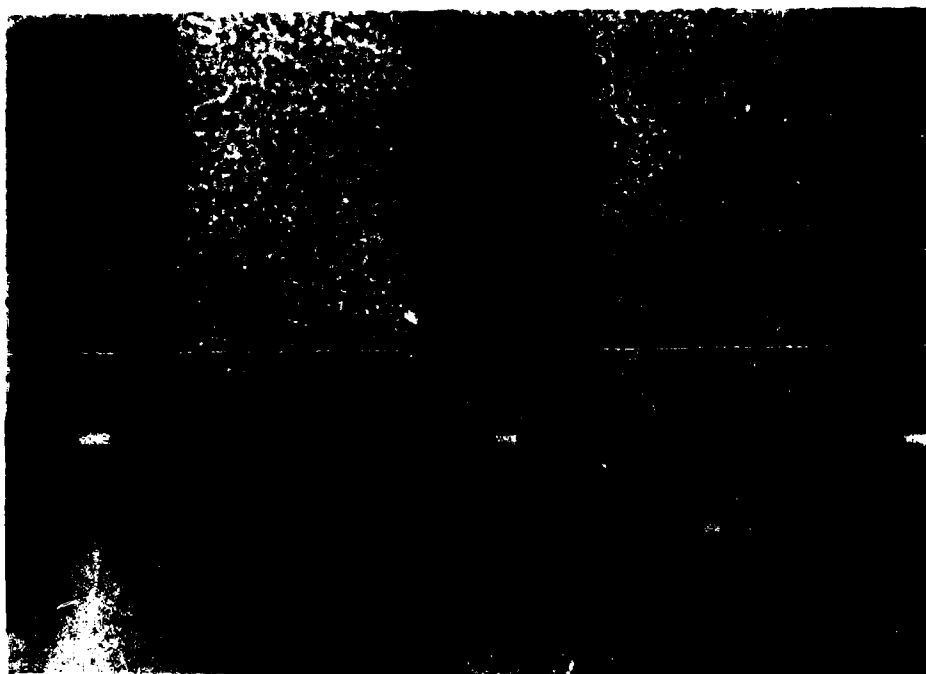
PHOTO 4 DETAIL OF COMPLETED VARACTOR REGION
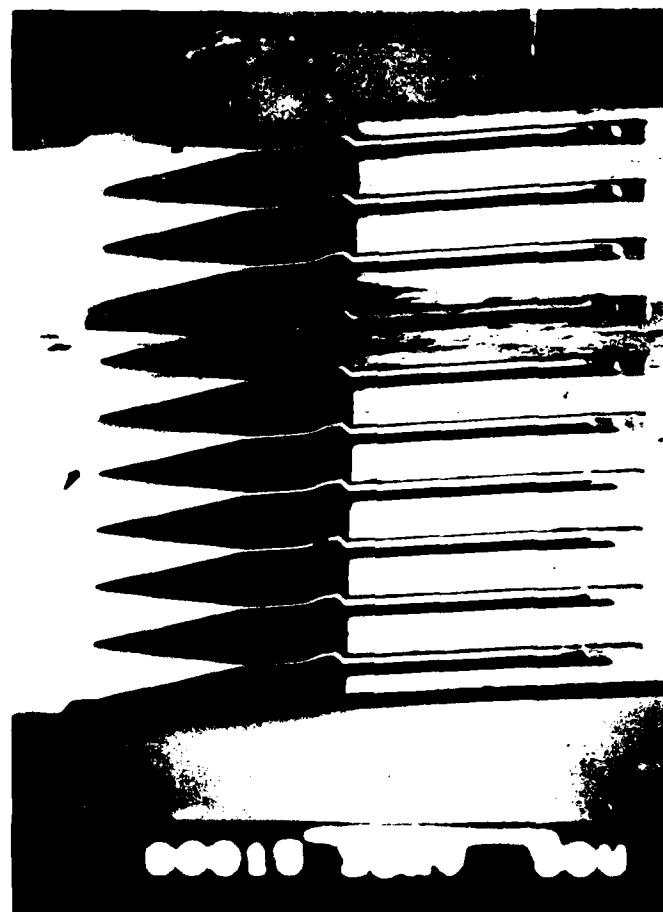
PHOTO 5   SEM PHOTOGRAPH OF COMPLETED VARACTOR REGION

PHOTO 6   SEM PHOTOGRAPH OF SINGLE VARACTOR FINGER
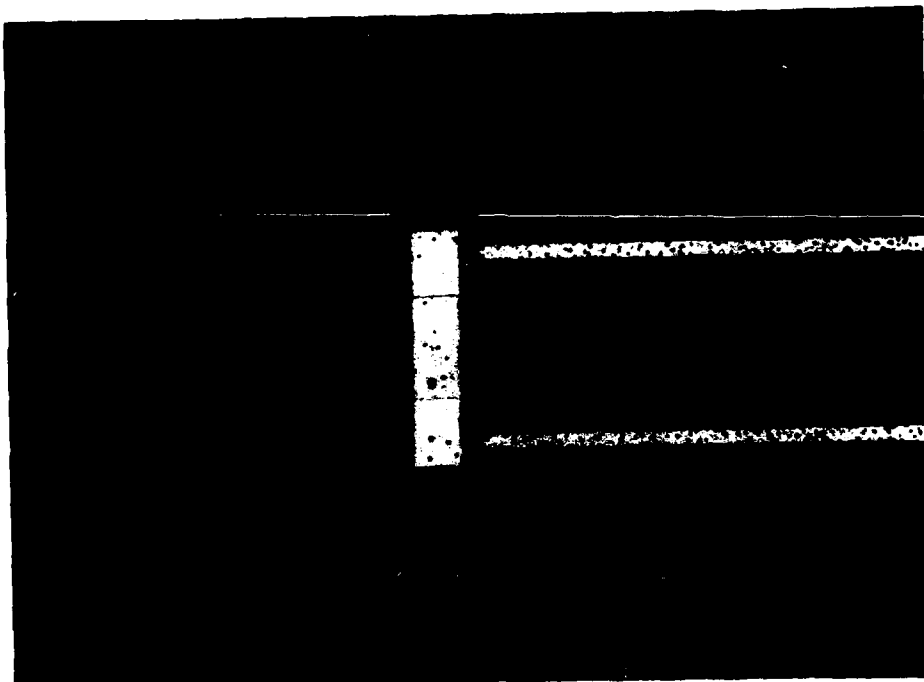
PHOTO 7 BIAS LINE DETAIL SHOWING RF BLOCK

PHOTO 8   SCHOTTKY PATTERN PRIOR TO METALLISATION SHOWING
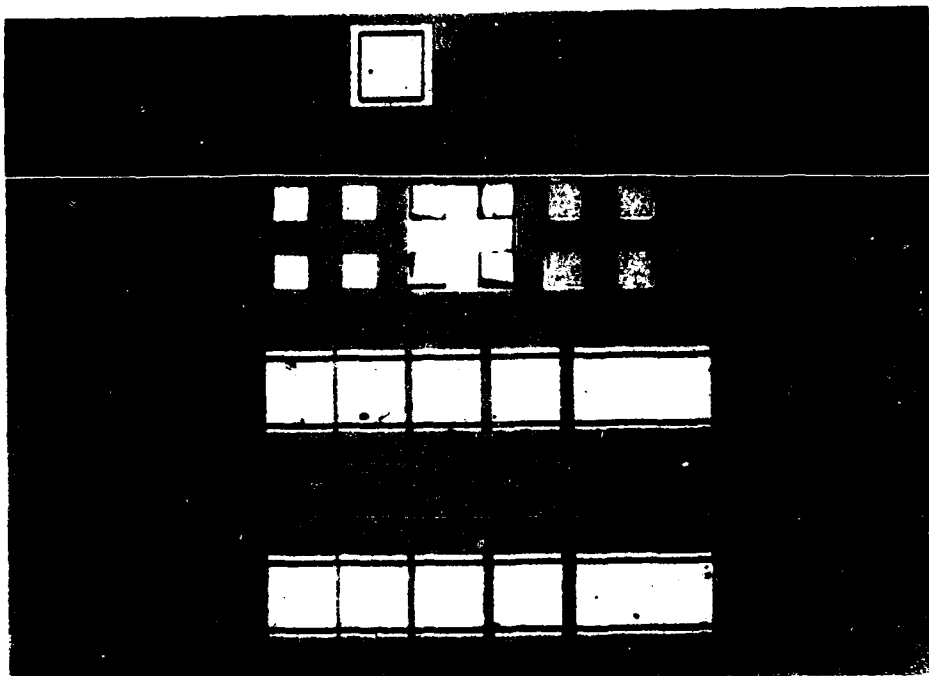ALIGNMENT AT FINGERS, DOORMAT AND MESA EDGES
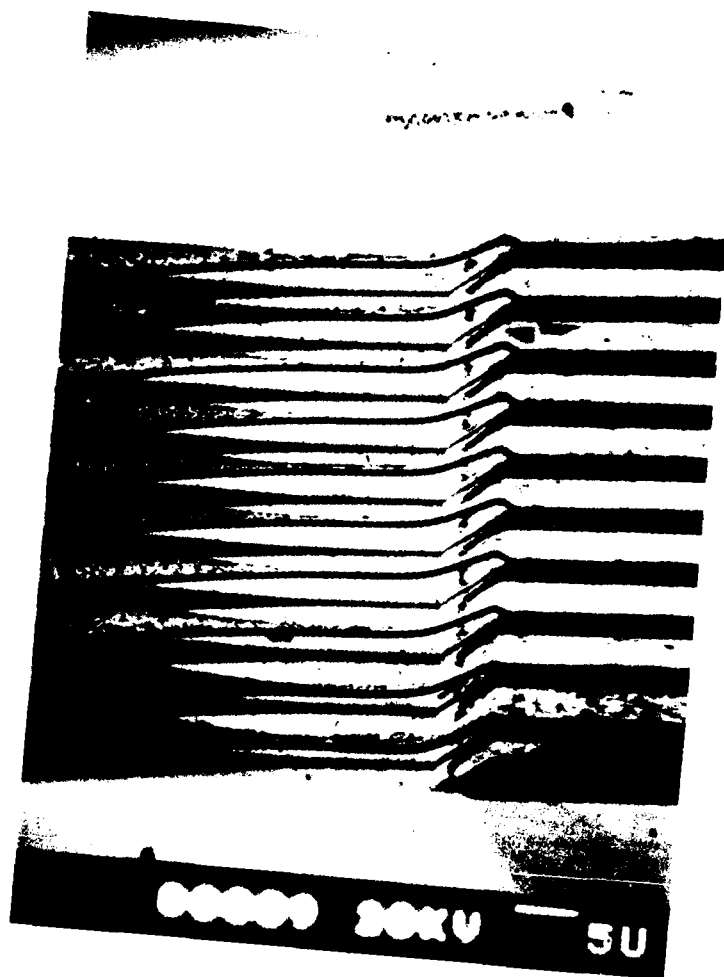
PHOTO 9   TRANSMISSION LINE OHMIC TEST PATTERN AND ALIGNMENT MARKS

PHOTO 10 "AIR BRIDGES" ON WAFER D

PHOTO 11   DETAIL OF "AIR BRIDGE" ON WAFER D
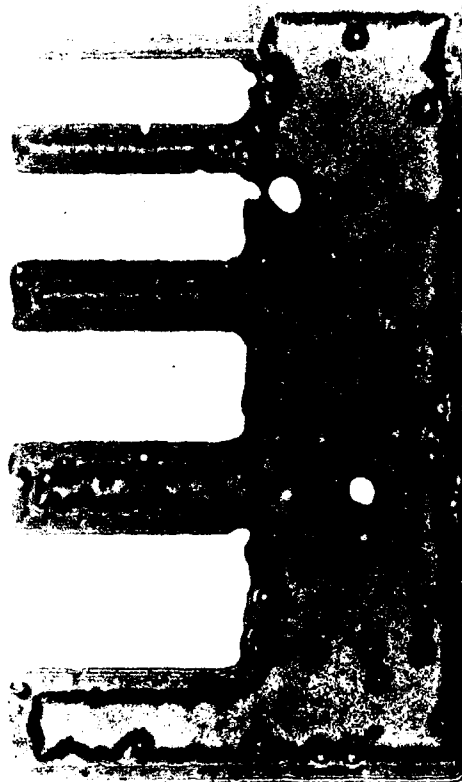
PHOTO 12   POLYIMIDE UNDERCUT TEST MASK

PHOTO 13   POLYIMIDE UNDERCUT USING STANDARD O_2 ASH
          CONDITIONS. (50 W, 150 cc/min), SLICE HORIZONTAL

**PHOTO 14 POLYIMIDE UNDERCUT USING STANDARD O$_2$ ASH
CONDITIONS. (50 W, 150 cc/min), SLICE VERTICAL**

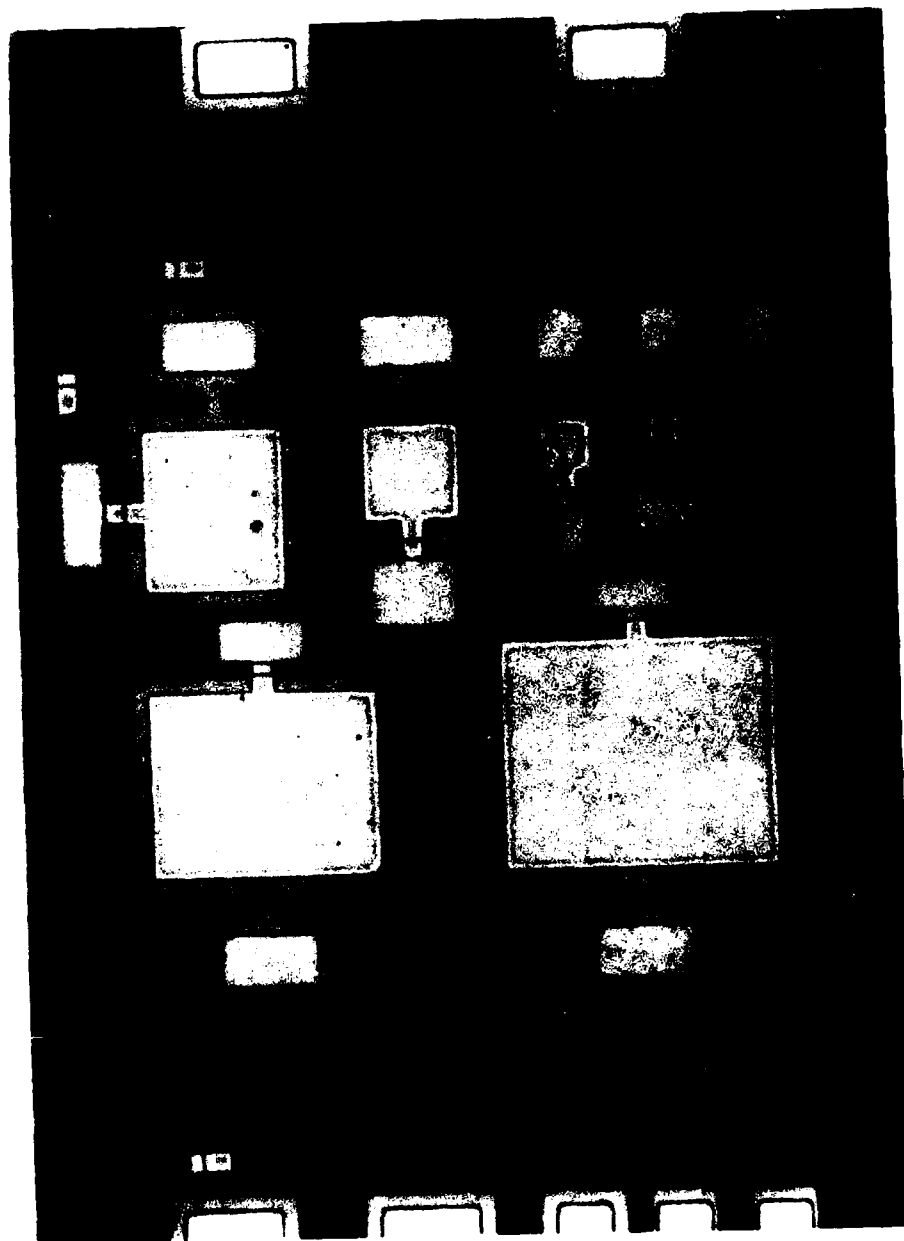**PHOTO 15   POLYIMIDE UNDERCUT USING LOW O$_2$FLOW RATE (50 W, 20 cc/min), SLICE VERTICAL**
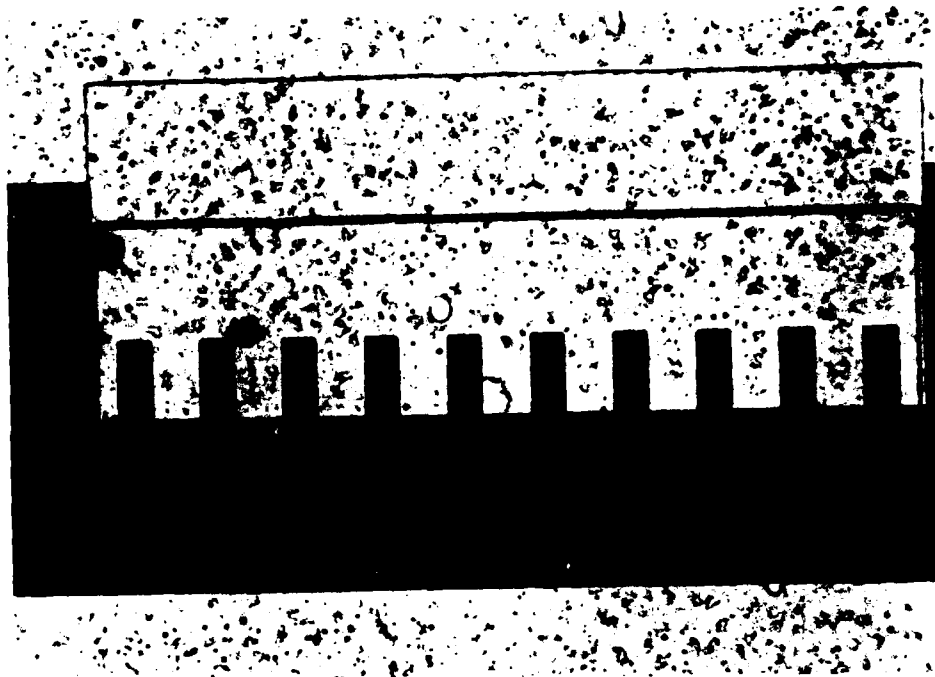
PHOTO 16   CAPACITOR TEST PATTERN

PHOTO 17   WAFER DURING PROCESSING, MASK 3 EXPOSED
AND METALLISED

END

DATE
FILMED

10-87